IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lin, et al

Examiner: Doan, Duc T.

Serial No: 10/008,872

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Title: MASTER TO MULTI-SLAVE ASYNCHRONOUS TRANSMIT FIFO

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REPLY TO EXAMINER'S ANSWER PURSUANT TO 37 C.F.R. § 41.41

Appellant submits this reply to the Examiner's Answer with a mailed date of June 17, 2008, and having a reply period ending two months from the date of the Examiner's Answer. 37 CFR § 41.41(a).

Claims 1, 3, 5,-7, 11-17, 20 and 22 were rejected under 35 USC 103(a) as being unpatentable over US Published App. No. 2002/0183013, to Auckland et al. ("Auckland"), in view of U.S. Patent No. 5,968,143, to Chisholm et al. ("Chisholm"), and further in view of U.S. Patent No. 6,434,630, to Micallizzi Jr. et al. ("Micallizzi").

Claim 21 was rejected under 35 USC 103(a) as being unpatentable over Auckland, Chisholm, Micallizzi as applied to claim 17, and in view of U.S. Published App. No. 2002/0009075 to Fesas, Jr. ("Fesas").

A. Rejections recited in the Final Office Action and repeated in the Examiner's Answer are improperly based upon a suggestion or motivation stemming from Appellant's claimed invention, and/or that the cited references fail to teach or suggest all the Appellant's claim limitations

Appellant respectfully submits that the Final Office Action and Examiner's Answer improperly bases the rejection of Appellant's claimed invention upon a motivation or suggestion stemming from Appellant's own claimed invention. That is, Appellant's own claimed invention is used as a blueprint for piecing together elements in the prior art to defeat patentability. *See In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998) (cited favorably by the post-*KSR International* opinion of *In re Translogic Technology, Inc.*, 504 F.3d 1249 (Fed. Cir. 2007)).

Also, Appellant respectfully submits that the reconfigurable analog RF front-end of Auckland, the dissimilar command block of Chisholm, and the SCSI command descriptor block of Micallizzi fail to teach or suggest all of the Appellant's claim limitations. Similarly, the further addition of the address translation device of Fesas to Appellant's claim 21 also fails to teach or suggest all of the Appellant's claim limitations. *See* MPEP § 2143.03 at page 2100-142 (Rev. 6, Sept. 2007) ("All words in a claim must be considered in judging the patentability of that claim against the prior art. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious."); *see also* MPEP § 2143 at 2100-118 ("[the Supreme Court] also recognized that [the teaching-suggestion-motivation (TSM) rationale] was one of a number of valid rationales that could be used to determine obviousness.").

"Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *See* 35 U.S.C. § 103(a). This legal construct is akin to the 'reasonable person' used as a reference in negligence determinations. The legal construct also presumes that all prior art references in the field of the invention are

available to this hypothetical skilled artisan. *See In re Carlson*, 983 F.2d 1032, 1038 (Fed. Cir. 1993)." *In re Rouffet* at 1357.

As noted by the Federal Circuit, "an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding *prior art corollaries* for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'" *Id.* (emphasis added).

In providing guidance "[t]o prevent the use of hindsight based on the invention to defeat patentability of the invention, [the Federal Circuit] requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, *confronted with the same problems as the inventor and with no knowledge of the claimed invention*, would select the elements from the cited prior art references for combination in the manner claimed." *Id.*

Appellant respectfully submits that its claimed invention improperly served as a blueprint fro piecing together elements from the cited references to defeat patentability. Appellant also respectfully submits that elements within the cited references do not teach or suggest the claim limitations as set out in Appellant's claimed invention.

1. Appellant's claimed invention relates generally to problems in resource allotment and transmission delays in wireless transmission environments

The present application 10/008,827 involves memory structure improvements addressing resource allotment and transmission delays present *in wireless transmission environments*, such as, for example, in master-to-multi-slave wireless transmission environments. (*See* Specification at p. 7, *ll.* 11-26 through p. 8, *ll.* 1-7).

Appellant's claimed invention is drawn to wireless transmission environments. Independent claim 1 relates to "a wireless transceiver device . . . ." Independent claim 7 relates to a method for storing and transmitting data . . . ." Independent claim 17 relates to "a memory structure formed within a baseband processing system . . . ."

Appellant's Specification recites, by way of example, that its "method is advantageous in that, when coupled with the described structures herein, it facilitates a FIFO architecture in a master-multi-slave environment in which the size of the FIFO structure is minimized because the FIFO structure is used to contain pointer addresses rather than actual blocks of data." (Specification at p. 16, *ll.* 4-19). For *re-transmission flexibility*, a "flexible structure is presented in which FIFO integrity or ordering may be achieved while minimizing the size of a FIFO memory structure." (Specification at p. 22, *ll.* 9-12).

Appellant's Figure 7 illustrates the memory structures "formed and configured according to the present invention. A random access memory 704 is configured to include at least three portions [of a data block portion 716, a command block portion 712, and an indicator portion 720]:"

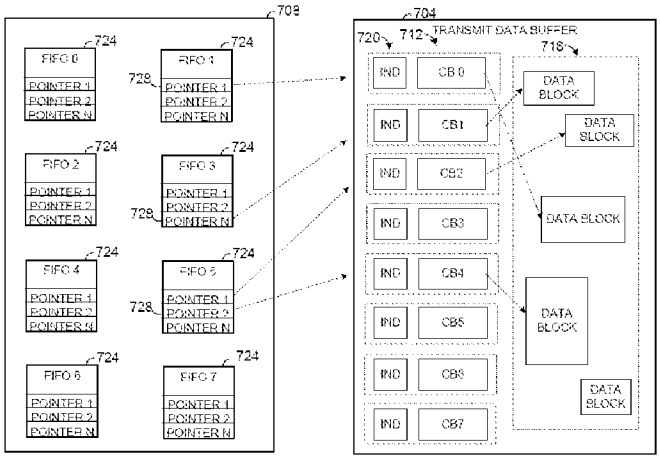

FIG. 7

(Specification at page 23, *ll.* 6-7). The FIFO structure 708 supports "the transmission of data blocks on a first in, first out basis. More specifically, random access memory 704 includes a command block portion 712 that is for storing command block. . . . A data block portion 716 includes actual data blocks that are to be transmitted. . . . [T]he data blocks are randomly distributed within the figure to suggest that the data blocks may be ordered in a random fashion. . . . An indicator portion 720 . . . is for storing a plurality of indicators . . . that identify whether a corresponding command block is *in use*. For example, command block 0 of portion 712 will have a one-bit indicator in for transmission purposes based upon the ordering of the command block pointer 608 that eventually corresponds to data block 3 stored in memory portion 648." (Specification at page 23, *ll.* 4-26, to page 24, *ll.* 1-3).

The term "'in use' refers to whether a transmission has been successfully completed for a corresponding data block stored in data block portion 716." (Specification at page 24, *ll.* 2-5). The "FIFO structure 708 [includes] a plurality of FIFO pointer blocks 724 [that] are used for specifying the order in which data blocks are to be transmitted." (Specification at page 24, *ll.* 11-13).

2. **Auckland** *was improperly cited for its related transceiver device because* **Auckland** *is directed towards a reconfigurable analog RF front-end and not data transmission techniques*

In the Examiner's Answer, Auckland is submitted as teaching that its "processor 614, as DSP or any general purpose processor, can be used to process data and instruction of any software routines of the radio . . . , and not necessarily limiting to just the [front-end] reconfiguration tasks for a variety of air interface standards . . . ." (Examiner's Answer at page 7).

In this regard, Auckland was cited for the transceiver elements; however, Auckland does not refer to data transmission methods or techniques, but simply "reconfigurable [RF hardware] for a variety of air interface standards." (Auckland ¶ 0048).

3. dissimilar command block of **Chisholm** *is distinguishable from the command block recited in Appellant's claimed invention*

In the Examiner's Answer, Chisholm is cited for "teaching command block/data structures with characteristics as claimed. The command/block data structures [of Chisholm] are used by a processor and software routine to execute the associating instructions and data, which are the same whether or not the environment is wireline or wireless." (Examiner's Answer at page 9).

From this argument, Appellant respectfully submits that its recited language is disregarded, and that the command block of Chisholm is improperly deemed a suitable corollary to replace that of Appellant's claimed invention.

As noted in Appellant's Appeal Brief, Chisholm recites that its command blocks pertain to command control between components of a personal computer. The disparate Chisholm command blocks do not include "addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use." (*see, e.g.,* Appellant's Claim 1; Specification at page 9, ll. 18-21).

Appellant also respectfully submits that the considerations of the same problems as the inventors encountered and/or addressed are summarily disregarded in the Examiner's Answer by equating wireline with wireless environments. As pointed to earlier, Appellant's claimed invention is direct towards the problems of resource allotment and transmission delays present in *wireless transmission environments*. Chisholm does not relate to wireless transmissions; nevertheless, the problems and solutions addressed in the Appellant's Specification were ignored.

The Examiner's Answer states that Chisholm "teaches . . . an indicator for indicating whether a command block . . . is in use." (Examiner's Answer at page 10). Chisholm does recite a "command transfer start signal into the host command address register set 311 which signals the command/data block transfer controller 209 to start a *command transfer* specified by the host address information." (Chisholm 5:30-34). As understood, the command transfer start signal is distinguishable from the indicator of Appellant's claimed invention, as Appellant's indicator is

for whether a command block is "in use," which refers to whether a transmission has been successfully completed for a corresponding data block stored in data block portion.

4. Examiner's Answer argues that it is irrelevant that SCSI command descriptor block device of **Micallizzi** *is directed towards interrupt management techniques instead of command blocks with addresses of data blocks and indicators for command blocks as recited in Appellant's claimed invention*

The Examiner's Answer states that Micalizzi was relied on for teaching a command block CDB having a pointer, the pointer pointing to "addresses of associating data segment/data blocks as claimed." (Examiner's Answer 10). As understood, Micalizzi was cited for its recitation of data pointers.

In Micalizzi, the "CDB" pointed to in the Examiner's Answer is a "SCSI command descriptor block (CDB) 118." SCSI is The SCSI CDB of Micallizzi "contains CDB bytes sent to the target or I/O device 80-86 during a COMMAND phase. The data segment address(es) 110, 114 is a starting address of a data segment stored in the memory 25 associated with a particular read or write I/O request." (Micalizzi 8:27-43). The acronym "SCSI" relates to "the second bus 70 [of Micallizzi, which] is a Small Computer Standard Interface (SCSI) bus [and not a wireless medium]." (Micallizzi 5:66-67).

Appellant respectfully submits that the CDB of Micallizzi are not command blocks with addresses of data blocks and indicators for command blocks as recited in Appellant's claimed invention, as set out above.

5. Fesas *recites address translation overhead reduction, not the use of command blocks with addresses of data blocks and indicators for command blocks in a wireless environment*

The Final Office Action noted that neither Auckland, Chisholm, nor Micallizzi recited specific command block lengths. In this regard, Fesas was cited as having a command block data structure having a length of 4 bytes.

Fesas relates to a "method and an apparatus for transferring data between a computer system and a network interface card that avoids virtual-to-physical address translations." (Fesas, Abstract). Fesas notes that the "advent of computer networking has given rise to devices that connect computer systems to packet-switched data networks. These devices . . . typically include interfaces to both the computer system and the packet-switched data network, as well as a buffer memory for buffering packets of data in transit between the computer system and the packet-switched data network." (Fesas ¶ 0004). In this regard, Fesas recites that "[w]hat is needed is performing DMA between a computer system and NIC which is free from the overhead of performing virtual to physical address translations . . . ." (Fesas ¶ 0009). Appellant respectfully submits that Fesas does not recite memory structure improvements addressing resource allotment and transmission delays present in wireless transmission environments.

B. Conclusion

The Examiner's Answer had summarily concluded that "it would have been obvious to one of ordinary skill in the art at the time of Appellant's invention to include the command block structure *as suggested* by [the host adaptor device of] Micalizzi in Auckland's [reconfigurable analog RF front-end] modified by [the command block transfer of] Chisholm." (Examiner's Answer at page 11).

In response, as supported above, Appellant respectfully submits that the Examiner's Answer disregards the problems and solutions proffered in Appellant's Specification, disregards the disparate methods and techniques set out in the cited references, and that the cited references *do not* teach or suggest all of Appellant's claim limitations. Further, Appellant respectfully submits that the elements cited in the Final Official Action and the Examiner's Answer serve, at most, as corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention.

Appellant respectfully submits that any motivation to combine the references improperly stem from improperly using Appellant's claimed invention as a blueprint for piecing together elements in the prior art to defeat patentability.

For the above-provided reasons, the Appellant respectfully requests that all of the rejections of the Final Office Action be overturned and that the claims in the present application be allowed to issue.

Respectfully submitted,

Date: July 21, 2008

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